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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SHEW, JOHN	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 12/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,729	CHEN ET AL.	
	Examiner	Art Unit	
	John L. Shew	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/29/2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-39* is/are rejected.

7)☒ Claim(s) *10,40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06032002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because

FIG. 2, referenced character "212B" needs to be added to identify "LINE CARD INTERCONNECT INTERFACE MODULE" of LINE CARD 202B .

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 3, 31, 32, 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Basso et al. (Pub. No. US 2002/0154634 A1).

Claim 1, Basso teaches a method comprising storing packet data within a storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers 505_1 – 505_5 to store packet data, maintaining a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by MultiCast Counter to determine when all instances have been transmitted, determining a release count value of said storage element (Fig.

5, page 5 para. [0084]-[0085]) referenced by the MCC release count of zero where the associated buffers 505_1 – 505_5 are returned to the free buffer queues, comparing said transmit count value and said release count value (Fig. 5, page 5 para. [0084]-[0085]) referenced by the comparison of the MCC to the value of zero, and de-allocating said storage element in response to comparing said transmit count value and said release count value (Fig. 5, page 5 para. [0084]-[0086]) referenced by the discard of Frame Control Block 501 and its associated buffers 505_1 – 505_5 by returning them to the free FCB and free buffer queues.

Claim 2, Basso teaches receiving a packet including said packet data (Fig. 2, page 3 para. [0059], page 4 para. [0060]) referenced by the reception of data packets from the Ethernet MAC interface 203 to the Dataflow chip 202, and allocating said storage element in response to receiving said packet (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 interfacing to a large Datastore Memory 205 for buffering of traffic.

Claim 3, Basso teaches transmitting said packet data from said storage element (Fig. 2, page 4 para. [0069]) referenced by the large Datastore Memory 205 as repository for frames awaiting retransmission and multiple DRAM interfaces to provide sustained transmit and receive bandwidth for the port interface.

Claim 31, Basso teaches a machine-readable medium (Fig. 3, page 4 para. [0060]-[0062]) referenced by the PowerPC microprocessor core 304 to interface with a SRAM instruction store , which when executed by a set of one or more processors (page 4 para. [0061]) referenced by the twelve Dyadic Protocol Processor Units, to perform operations comprising storing packet data within a storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers 505_1 – 505_5 to store packet data, maintaining a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by MultiCast Counter to determine when all instances have been transmitted, determining a release count value of said storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by the MCC release count of zero where the associated buffers 505_1 – 505_5 are returned to the free buffer queues, comparing said transmit count value and said release count value (Fig. 5, page 5 para. [0084]-[0085]) referenced by the comparison of the MCC to the value of zero, and de-allocating said storage element in response to comparing said transmit count value and said release count value (Fig. 5, page 5 para. [0084]-[0086]) referenced by the discard of Frame Control Block 501 and its associated buffers 505_1 – 505_5 by returning them to the free FCB and free buffer queues.

Claim 32, Basso teaches said operations further comprising receiving a packet including said packet data (Fig. 2, page 3 para. [0059], page 4 para. [0060]) referenced by the reception of data packets from the Ethernet MAC interface 203 to the Dataflow chip 202, and allocating said storage element in response to receiving said packet (Fig. 2,

page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 interfacing to a large Datastore Memory 205 for buffering of traffic.

Claim 33, Basso teaches said operations further comprising transmitting said packet data from said storage element (Fig. 2, page 4 para. [0069]) referenced by the large Datastore Memory 205 as repository for frames awaiting retransmission and multiple DRAM interfaces to provide sustained transmit and receive bandwidth for the port interface.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 5, 6, 7, 9, 11, 12, 13, 14, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 30, 34, 35, 36, 37, 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Basso as applied to claims 1-3, 31-33 above, in view of Gulick (Patent No. 4809269).

Claim 4, Busso teaches wherein maintaing a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by MultiCast Counter to determine when all instances have been transmitted, comprises initializing said transmit count value (Fig. 5, page 5 para. [0084]-[0085, page 6 para. [0104]-[0106]) referenced by MultiCast Counter value stored by the Dataflow Chip based on the multicast action. Busso does not teach incrementing said transmit count value by one in response to transmitting said packet data.

Gulick teaches incrementing said transmit count value by one in response to transmitting said packet data (Fig. 5, col. 10 lines 29-58) referenced by the Transmit Byte Counter 154 receiving a COUNT signal upon a Transmit FIFO buffer 150 output and comparison of the Transmit Byte Counter 154 to a Threshold Comparison Logic 158 to determine if the end count threshold is reached.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Dual Port Timing Controller of Gulick to the Multicast Data Structure of Basso for the purpose of providing control signals allowing ordinary RAM to be operated as an S-RAM as suggested by Gulick (col. 1 lines 57-60).

Claim 5, Busso teaches wherein comparing said transmit count value and said release count value (Fig. 5, page 5 para. [0084]-[0085]) referenced by the comparison of the MCC to the value of zero, comprises de-allocating said storage element in response to comparing said transmit count value and said release count value (Fig. 5, page 5 para. [0084]-[0086]) referenced by the discard of Frame Control Block 501 and its associated

buffers 505_1 – 505_5 by returning them to the free FCB and free buffer queues. Basso does not teach the determining whether an incremented transmit count value is equal to a release count value

Gulick teaches determining whether an incremented transmit count value is equal to a release count value (Fig. 5, col. 10 lines 29-58) referenced by the Transmit Byte Counter 154 is compared to the Threshold Comparison Logic 158 to determine if the threshold count is reached.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Dual Port Timing Controller of Gulick to the Multicast Data Structure of Basso for the purpose of providing control signals allowing ordinary RAM to be operated as an S-RAM as suggested by Gulick (col. 1 lines 57-60).

Claim 6, Busso teaches wherein transmitting said packet data from said storage element (Fig. 2, page 4 para. [0069]) referenced by the large Datastore Memory 205 as repository for frames awaiting retransmission and multiple DRAM interfaces to provide sustained transmit and receive bandwidth for the port interface, comprises transmitting said packet data from said storage element via a plurality of output interfaces (Fig. 2, Fig. 5, page 5 para. [0084]-[0086]) referenced by the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports.

Claim 7, Busso teaches wherein transmitting said packet data from said storage element (Fig. 2, page 4 para. [0068]-[0069]) referenced by the large Datastore Memory 205 as repository for frames awaiting retransmission and multiple DRAM interfaces to provide sustained transmit and receive bandwidth for the port interface, via a plurality of output interfaces (Fig. 2, Fig. 5, page 5 para. [0084]-[0086]) referenced by the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports, comprises transmitting said packet data from said storage element via a plurality of line interfaces (Fig. 2, page 4 para. [0068]-[0069]) referenced by the interconnections between the Data Store 205 and the Dataflow chip 202 and ultimate transfer to the Ethernet MAC 203.

Claim 9, Busso teaches said packet data including a packet header (Fig. 4, page 5 para. [0075]-[0083]) referenced by the Message ID and Message Parameters, and a packet body (Fig. 4, page 5 para. [0075]-[0083]) referenced by the Data, wherein storing packet data within a storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers 505_1 – 505_5 to store packet data, comprises storing said packet body within a common storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers 505_1 – 505_5 to store packet data, storing a copy of said packet header within a unique storage element for each of said plurality of output interfaces (Fig. 5, page 6 para. [0090]) referenced by the unique data for the instance written to the Frame Alteration Control Block 503 for different header data to different output ports, and associating

each of said plurality of unique storage elements with said common storage element (Fig. 5) referenced by the linkage of the FACB 503 to the Buffers $505_1 - 505_5$.

Claim 11, Busso teaches an input module to store packet data within a storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the reception of data packets from the input Ethernet MAC interface 203 to the Dataflow chip 202 which interfaces to a large Datastore Memory 205 for buffering of traffic, and to initialize a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085, page 6 para. [0104]-[0106]) referenced by MultiCast Counter value stored by the Dataflow Chip based on the multicast action, a processing element to determine a release count value of said storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by the Dataflow chip 202 comparing the MCC release count of zero where the associated buffers $505_1 - 505_5$ are returned to the free buffer queues, a direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, and to de-allocate said storage element in response to a determination that said transmit count value is equal to said release count value (Fig. 5, page 5 para. [0084]-[0086]) referenced by the comparison of the MCC to the value of zero followed by the discard of Frame Control Block 501 and its associated buffers $505_1 - 505_5$ by returning them to the free FCB and free buffer queues. Busso does not teach a memory controller to increment said transmit count value by one in response to a transmission of said packet data.

Gulick teaches a controller incrementing said transmit count value by one in response to transmitting said packet data (Fig. 5, col. 10 lines 29-58) referenced by the Transmit Byte Counter 154 receiving a COUNT signal upon a Transmit FIFO buffer 150 output and comparison of the Transmit Byte Counter 154 to a Threshold Comparison Logic 158 to determine if the end count threshold is reached.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Dual Port Timing Controller of Gulick to the Multicast Data Structure of Basso for the purpose of providing control signals allowing ordinary RAM to be operated as an S-RAM as suggested by Gulick (col. 1 lines 57-60).

Claim 12, Busso teaches wherein said input module to store packet data within a storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the reception of data packets from the input Ethernet MAC interface 203 to the Dataflow chip 202 which interfaces to a large Datastore Memory 205 for buffering of traffic, and to initialize a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085, page 6 para. [0104]-[0106]) referenced by MultiCast Counter value stored by the Dataflow Chip based on the multicast action, comprises an input module to receive a packet including said packet data (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203, including said packet data (Fig. 4) referenced by the message Data, and to allocate said storage element for said packet including said packet data (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 interfacing to a large Datastore Memory 205 for buffering of traffic.

Claim 13, Busso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, comprises a direct memory access controller to transmit said packet data from said storage element via a plurality of output interfaces (Fig. 2, Fig. 5, page 5 para. [0084]-[0086]) referenced by the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports.

Claim 14, Busso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, via a plurality of output interfaces (Fig. 2, Fig. 5, page 5 para. [0084]-[0086]) referenced by the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports, comprises a direct memory access controller to transmit said packet data from said storage element via a plurality of line interfaces (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 of various transmission protocol rates.

Claim 16, Busso teaches said packet data including a packet header (Fig. 4, page 5 para. [0075]-[0083]) referenced by the Message ID and Message Parameters, and a packet body (Fig. 4, page 5 para. [0075]-[0083]) referenced by the Data, wherein said input module to store packet data within a storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the reception of data packets from the input Ethernet MAC interface 203 to the Dataflow chip 202 which interfaces to a large Datastore Memory 205 for buffering of traffic, and to initialize a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085, page 6 para. [0104]-[0106]) referenced by MultiCast Counter value stored by the Dataflow Chip based on the multicast action, comprises an input module to store said packet body within a common storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers $505_1 - 505_5$ to store packet data, and said processing element to determine a release count value of said storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by the Dataflow determining the MCC release count of zero where the associated buffers $505_1 - 505_5$ are returned to the free buffer queues, comprises a processing element to store a copy of said packet header within a unique storage element for each of said plurality of output interfaces (Fig. 5, page 6 para. [0090]) referenced by the unique data for the instance written to the Frame Alteration Control Block 503 for different header data to different output ports, and to associate each of said plurality of unique storage elements with said common storage element (Fig. 5) referenced by the linkage of the FACB 503 to the Buffers $505_1 - 505_5$.

Claim 17, Busso teaches an apparatus comprising a first line card to transmit data to a communications network (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203, a line card interconnect coupled to said first line card and a second line card coupled to said line card interconnect (Fig. 2, page 3 para. [0059]) referenced by the interconnection between the Ethernet MAC interface 203 and the Dataflow Chip 202, to receive data from a communications network (Fig. 2, page 3 para. [0059], page 4 para. [0060]) referenced by the Dataflow Chip 202 transmitting and receiving traffic via network port, said second line card including an input module to store packet data within a storage element (FIG. 2, page 3 para. [0059], page 4 para. [0060]) referenced by the Embedded Processor Complex 209 to control the data storage through lookup tables and processing of headers, and to initialize a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085], page 6 para. [0106]) referenced by the MultiCast Counter whose value is assigned by the Dataflow Chip 202, a processing element to determine a release count value of said storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by the Dataflow chip 202 comparing the MCC release count of zero where the associated buffers 505_1 – 505_5 are returned to the free buffer queues, a direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, and to de-allocate said storage element in response to a determination that said transmit count value is equal to said release count value (Fig. 5, page 5 para. [0084]-[0086]) referenced by the comparison of the MCC to the value of

zero followed by the discard of Frame Control Block 501 and its associated buffers 505_1 – 505_5 by returning them to the free FCB and free buffer queues. Busso does not teach a memory controller to increment said transmit count value by one in response to a transmission of said packet data.

Gulick teaches a controller incrementing said transmit count value by one in response to transmitting said packet data (Fig. 5, col. 10 lines 29-58) referenced by the Transmit Byte Counter 154 receiving a COUNT signal upon a Transmit FIFO buffer 150 output and comparison of the Transmit Byte Counter 154 to a Threshold Comparison Logic 158 to determine if the end count threshold is reached.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Dual Port Timing Controller of Gulick to the Multicast Data Structure of Basso for the purpose of providing control signals allowing ordinary RAM to be operated as an S-RAM as suggested by Gulick (col. 1 lines 57-60).

Claim 18, Busso teaches said second line card (Fig. 2, page 3 para. [0059]) referenced by the Dataflow Chip 202, further including a line interface module to receive data from a communications network (Fig. 2, page 3 para. [0059]) referenced by the Dataflow chip 202 interface to the Ethernet MAC interface 203, wherein said input module to store packet data within a storage element (FIG. 2, page 3 para. [0059], page 4 para. [0060]) referenced by the Embedded Processor Complex 209 to control the data storage through lookup tables and processing of headers, and to initialize a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085], page 6 para. [0106])

referenced by the MultiCast Counter whose value is assigned by the Dataflow Chip 202, comprises an input module to receive a packet including said packet data from said line interface module (Fig. 2, page 3 para. [0059], page 4 para. [0060]-[0061]) referenced by the Embedded Processor Complex 209 receiving packet data from the Ethernet MAC interface 203 for table lookup with the Dataflow chip 202 storing the packet in the Datastore Memory 205, and to allocate said storage element for said packet including said packet data (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers 505_1 – 505_5 allocatated to store packet data.

Claim 19, Busso teaches said second line card (Fig. 2, page 3 para. [0059]) referenced by the Dataflow Chip 202, further including a memory coupled to said memory controller to store said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which acts as a memory controller to transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203.

Claim 20, Busso teaches said second line card (Fig. 2, page 3 para. [0059]) referenced by the Dataflow Chip 202, further including a line card interconnect interface module having a plurality of output interfaces coupled to said line card interconnect (Fig. 2, page 3 para. [0059]) referenced by the Dataflow Chip 202 interconnection with the Ethernet MAC interface 203 which carries a plurality of output ports including 1xOC-192c 4xOC-48c 16xOC-12c 1x10Gb Ethernet and 10x1Gb Ethernet.

Claim 21, Busso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, comprises a direct memory access controller to transmit said packet data from said storage element to said line card interconnect interface module (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203 through the interconnection between the Dataflow chip 202 and the Ethernet MAC interface 203.

Claim 22, Busso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, comprises a direct memory access controller to transmit said packet data from said storage element via a plurality of output interfaces (Fig. 2, Fig. 5, page 5 para. [0084]-[0086]) referenced by the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports.

Claim 23, Busso teaches said packet data including a packet header (Fig. 4, page 5 para. [0075]-[0083]) referenced by the Message ID and Message Parameters, and a packet body (Fig. 4, page 5 para. [0075]-[0083]) referenced by the Data, wherein said

input module to store packet data within a storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the reception of data packets from the input Ethernet MAC interface 203 to the Dataflow chip 202 which interfaces to a large Datastore Memory 205 for buffering of traffic, and to initialize a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085, page 6 para. [0104]-[0106]) referenced by MultiCast Counter value stored by the Dataflow Chip based on the multicast action, comprises an input module to store said packet body within a common storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers 505_1 – 505_5 to store packet data, and said processing element to determine a release count value of said storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by the Dataflow determining the MCC release count of zero where the associated buffers 505_1 – 505_5 are returned to the free buffer queues, comprises a processing element to store a copy of said packet header within a unique storage element for each of said plurality of output interfaces (Fig. 5, page 6 para. [0090]) referenced by the unique data for the instance written to the Frame Alteration Control Block 503 for different header data to different output ports, and to associate each of said plurality of unique storage elements with said common storage element (Fig. 5) referenced by the linkage of the FACB 503 to the Buffers 505_1 – 505_5.

Claim 24, Busso teaches an apparatus comprising a first line card to transmit data to a communications network (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203, a line card interconnect coupled to said first line card and a second line

card coupled to said line card interconnect (Fig. 2, page 3 para. [0059]) referenced by the interconnection between the Ethernet MAC interface 203 and the Dataflow Chip 202, to transmit data to a communications network (Fig. 2, page 3 para. [0059], page 4 para. [0060]) referenced by the Dataflow Chip 202 transmitting and receiving traffic via network port, said second line card including an input module to store packet data within a storage element (FIG. 2, page 3 para. [0059], page 4 para. [0060]) referenced by the Embedded Processor Complex 209 to control the data storage through lookup tables and processing of headers, and to initialize a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085], page 6 para. [0106]) referenced by the MultiCast Counter whose value is assigned by the Dataflow Chip 202, a processing element to determine a release count value of said storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by the Dataflow chip 202 comparing the MCC release count of zero where the associated buffers 505_1 – 505_5 are returned to the free buffer queues, a direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, and to de-allocate said storage element in response to a determination that said transmit count value is equal to said release count value (Fig. 5, page 5 para. [0084]-[0086]) referenced by the comparison of the MCC to the value of zero followed by the discard of Frame Control Block 501 and its associated buffers 505_1 – 505_5 by returning them to the free FCB and free buffer queues. Busso does not teach

a memory controller to increment said transmit count value by one in response to a transmission of said packet data.

Gulick teaches a controller incrementing said transmit count value by one in response to transmitting said packet data (Fig. 5, col. 10 lines 29-58) referenced by the Transmit Byte Counter 154 receiving a COUNT signal upon a Transmit FIFO buffer 150 output and comparison of the Transmit Byte Counter 154 to a Threshold Comparison Logic 158 to determine if the end count threshold is reached.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Dual Port Timing Controller of Gulick to the Multicast Data Structure of Basso for the purpose of providing control signals allowing ordinary RAM to be operated as an S-RAM as suggested by Gulick (col. 1 lines 57-60).

Claim 25, Busso teaches said second line card (Fig. 2, page 3 para. [0059]) referenced by the Dataflow Chip 202, further including a line card interconnect interface module coupled to said line card interconnect (Fig. 2, page 3 para. [0059]) referenced by the interconnection of Dataflow chip 202 and the Ethernet MAC interface 203, wherein said input module to store packet data within a storage element (FIG. 2, page 3 para. [0059], page 4 para. [0060]) referenced by the Embedded Processor Complex 209 to control the data storage through lookup tables and processing of headers, and to initialize a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085], page 6 para. [0106]) referenced by the MultiCast Counter whose value is assigned by the Dataflow Chip 202, comprises an input module to receive a packet including said packet

data from said line card connect interface module (Fig. 2, page 3 para. [0059], page 4 para. [0060]-[0061]) referenced by the Embedded Processor Complex 209 receiving packet data from the interconnection to the Ethernet MAC interface 203 for table lookup with the Dataflow chip 202 storing the packet in the Datastore Memory 205, and to allocate said storage element for said packet including said packet data (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers $505_1 - 505_5$ allocatated to store packet data.

Claim 26, Busso teaches said second line card (Fig. 2, page 3 para. [0059]) referenced by the Dataflow Chip 202, further including a memory coupled to said memory controller to store said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which acts as a memory controller to transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203.

Claim 27, Busso teaches said second line card (Fig. 2, page 3 para. [0059]) referenced by the Dataflow Chip 202, further including a line interface module having a plurality of output interfaces (Fig. 2, page 3 para. [0059]) referenced by the Dataflow Chip 202 interconnection with the Ethernet MAC interface 203 which carries a plurality of output ports including 1xOC-192c 4xOC-48c 16xOC-12c 1x10Gb Ethernet and 10x1Gb Ethernet.

Claim 28, Busso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para.

[0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, comprises a direct memory access controller to transmit said packet data from said storage element via said plurality of output interfaces (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203 which has a plurality of output ports including 1xOC-192c 4xOC-48c 16xOC-12c 1x10Gb Ethernet and 10x1Gb Ethernet.

Claim 30, Busso teaches said packet data including a packet header (Fig. 4, page 5 para. [0075]-[0083]) referenced by the Message ID and Message Parameters, and a packet body (Fig. 4, page 5 para. [0075]-[0083]) referenced by the Data, wherein said input module to store packet data within a storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the reception of data packets from the input Ethernet MAC interface 203 to the Dataflow chip 202 which interfaces to a large Datastore Memory 205 for buffering of traffic, and to initialize a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085, page 6 para. [0104]-[0106]) referenced by MultiCast Counter value stored by the Dataflow Chip based on the multicast action, comprises an input module to store said packet body within a common storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers 505_1 – 505_5 to store packet data, and said processing element to determine a release count value of said storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by the Dataflow determining the MCC release count of zero where the associated buffers 505_1 – 505_5

are returned to the free buffer queues, comprises a processing element to store a copy of said packet header within a unique storage element for each of said plurality of output interfaces (Fig. 5, page 6 para. [0090]) referenced by the unique data for the instance written to the Frame Alteration Control Block 503 for different header data to different output ports, and to associate each of said plurality of unique storage elements with said common storage element (Fig. 5) referenced by the linkage of the FACB 503 to the Buffers 505_1 – 505_5.

Claim 34, Busso teaches wherein maintaing a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by MultiCast Counter to determine when all instances have been transmitted, comprises initializing said transmit count value (Fig. 5, page 5 para. [0084]-[0085, page 6 para. [0104]-[0106]) referenced by MultiCast Counter value stored by the Dataflow Chip based on the multicast action. Busso does not teach incrementing said transmit count value by one in response to transmitting said packet data.

Gulick teaches incrementing said transmit count value by one in response to transmitting said packet data (Fig. 5, col. 10 lines 29-58) referenced by the Transmit Byte Counter 154 receiving a COUNT signal upon a Transmit FIFO buffer 150 output and comparison of the Transmit Byte Counter 154 to a Threshold Comparison Logic 158 to determine if the end count threshold is reached.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Dual Port Timing Controller of Gulick to the Multicast Data

Structure of Basso for the purpose of providing control signals allowing ordinary RAM to be operated as an S-RAM as suggested by Gulick (col. 1 lines 57-60).

Claim 35, Busso teaches wherein comparing said transmit count value and said release count value (Fig. 5, page 5 para. [0084]-[0085]) referenced by the comparison of the MCC to the value of zero, comprises de-allocating said storage element in response to comparing said transmit count value and said release count value (Fig. 5, page 5 para. [0084]-[0086]) referenced by the discard of Frame Control Block 501 and its associated buffers 505_1 – 505_5 by returning them to the free FCB and free buffer queues. Basso does not teach the determining whether an incremented transmit count value is equal to a release count value

Gulick teaches determining whether an incremented transmit count value is equal to a release count value (Fig. 5, col. 10 lines 29-58) referenced by the Transmit Byte Counter 154 is compared to the Threshold Comparison Logic 158 to determine if the threshold count is reached.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Dual Port Timing Controller of Gulick to the Multicast Data Structure of Basso for the purpose of providing control signals allowing ordinary RAM to be operated as an S-RAM as suggested by Gulick (col. 1 lines 57-60).

Claim 36, Busso teaches wherein transmitting said packet data from said storage element (Fig. 2, page 4 para. [0069]) referenced by the large Datastore Memory 205 as

repository for frames awaiting retransmission and multiple DRAM interfaces to provide sustained transmit and receive bandwidth for the port interface, comprises transmitting said packet data from said storage element via a plurality of output interfaces (Fig. 2, Fig. 5, page 5 para. [0084]-[0086]) referenced by the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports.

Claim 37, Busso teaches wherein transmitting said packet data from said storage element (Fig. 2, page 4 para. [0068]-[0069]) referenced by the large Datastore Memory 205 as repository for frames awaiting retransmission and multiple DRAM interfaces to provide sustained transmit and receive bandwidth for the port interface, via a plurality of output interfaces (Fig. 2, Fig. 5, page 5 para. [0084]-[0086]) referenced by the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports, comprises transmitting said packet data from said storage element via a plurality of line interfaces (Fig. 2, page 4 para. [0068]-[0069]) referenced by the interconnections between the Data Store 205 and the Dataflow chip 202 and ultimate transfer to the Ethernet MAC 203.

Claim 39, Busso teaches said packet data including a packet header (Fig. 4, page 5 para. [0075]-[0083]) referenced by the Message ID and Message Parameters, and a packet body (Fig. 4, page 5 para. [0075]-[0083]) referenced by the Data, wherein storing packet data within a storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by

Buffers 505_1 – 505_5 to store packet data, comprises storing said packet body within a common storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers 505_1 – 505_5 to store packet data, storing a copy of said packet header within a unique storage element for each of said plurality of output interfaces (Fig. 5, page 6 para. [0090]) referenced by the unique data for the instance written to the Frame Alteration Control Block 503 for different header data to different output ports, and associating each of said plurality of unique storage elements with said common storage element (Fig. 5) referenced by the linkage of the FACB 503 to the Buffers 505_1 – 505_5.

4. Claims 8, 15, 28, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Busso and Gulick as applied to claims 1-4, 5, 6, 7, 9, 11, 12, 13, 14, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 30, 31-34, 35, 36, 37above, and further in view of Chow et al. (Patent No. US 6269081).

Claim 8, Busso teaches wherein transmitting said packet data from said storage element (Fig. 2, page 4 para. [0068]-[0069]) referenced by the large Datastore Memory 205 as repository for frames awaiting retransmission and multiple DRAM interfaces to provide sustained transmit and receive bandwidth for the port interface, via a plurality of line interfaces (Fig. 2, page 4 para. [0068]-[0069], Fig. 5, page 5 para. [0084]-[0086])

referenced by the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports and by the interconnections between the Data Store 205 and the Dataflow chip 202 with ultimate transfer to the Ethernet MAC 203, comprises transmitting said packet data from said storage element via a line interface (Fig. 2, page 4 para. [0068]-[0069]) referenced by the interconnections between the Data Store 205 and the Dataflow chip 202 and ultimate transfer to the Ethernet MAC 203, selected from the group consisting of an Ethernet interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203, a Fast Ethernet Interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 with 10Gb Ethernet, a Gigabit Ethernet interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 with 10x1Gb Ethernet, an OC-48/STM-16 interface (Fig. 2, page 3 para. [0059]) referenced by the Packet Over Sonet interface 203 with 4xOC-48c, an OC-12/STM-14 interface (Fig. 2, page 3 para. [0059]) referenced by the Packet Over Sonet interface 203 with 16xOC-12c, an OC-3/STM-1. Busso and Gulick do not teach an OC-3/STM-1 interface, an IF Video interface, a DS-1 interface, a DS-3 interface, an E-1 interface and an E-3 interface.

Chow teaches an OC-3/STM-1 interface (Fig. 1, col. 6 lines 7-45) referenced by the OC-3 of 1.6 Gbps Access Shelf 3B, an IF Video interface (Fig. 1, col. 6 lines 7-45) referenced by the FastBus Video of 800Mbps Access Shelf 3C, a DS-1 interface (Fig. 1, col. 6 lines 7-45) referenced by DS-1 of 800Mbps Access Shelf 3D, a DS-3 interface (Fig. 1, col. 6 lines 7-45) referenced by the DS-3 of 800Mbps Access Shelf 3C, an E-1

interface (Fig. 1, col. 6 lines 7-45) referenced by the E-1 of 800Mbps Access Shelf 3D, and an E-3 interface (Fig. 1, col. 6 lines 7-45) referenced by the E-3 of 800Mbps Access Shelf 3C.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Switching Core interfaces of Chowto the Multicast Data Structure of Basso and Gulick for the purpose of maximizing utilization of a switching core by providing a variable number of universal card slots depending on the interface card bandwidth as suggested by Chow (col. 4 lines 50-54).

Claim 15, Busso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, via a plurality of line interfaces (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 of various transmission protocol rates, comprises a direct memory access controller to transmit said packet data from said storage element via a line interface (Fig. 2, page 4 para. [0068]-[0069]) referenced by the interconnections between the Data Store 205 and the Dataflow chip 202 and ultimate transfer to the Ethernet MAC 203, selected from the group consisting of an Ethernet interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203, a Fast Ethernet Interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 with 10Gb Ethernet, a Gigabit Ethernet interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203

with 10x1Gb Ethernet, an OC-48/STM-16 interface (Fig. 2, page 3 para. [0059]) referenced by the Packet Over Sonet interface 203 with 4xOC-48c, an OC-12/STM-14 interface (Fig. 2, page 3 para. [0059]) referenced by the Packet Over Sonet interface 203 with 16xOC-12c. Busso and Gulick do not teach an OC-3/STM-1 interface, an IF Video interface, a DS-1 interface, a DS-3 interface, an E-1 interface and an E-3 interface.

Chow teaches an OC-3/STM-1 interface (Fig. 1, col. 6 lines 7-45) referenced by the OC-3 of 1.6 Gbps Access Shelf 3B, an IF Video interface (Fig. 1, col. 6 lines 7-45) referenced by the FastBus Video of 800Mbps Access Shelf 3C, a DS-1 interface (Fig. 1, col. 6 lines 7-45) referenced by DS-1 of 800Mbps Access Shelf 3D, a DS-3 interface (Fig. 1, col. 6 lines 7-45) referenced by the DS-3 of 800Mbps Access Shelf 3C, an E-1 interface (Fig. 1, col. 6 lines 7-45) referenced by the E-1 of 800Mbps Access Shelf 3D, and an E-3 interface (Fig. 1, col. 6 lines 7-45) referenced by the E-3 of 800Mbps Access Shelf 3C.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Switching Core interfaces of Chowto the Multicast Data Structure of Basso and Gulick for the purpose of maximizing utilization of a switching core by providing a variable number of universal card slots depending on the interface card bandwidth as suggested by Chow (col. 4 lines 50-54).

Claim 29, Busso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para.

[0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, via a plurality of output (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 of various ports carrying different transmission protocol rates, comprises a direct memory access controller to transmit said packet data from said storage element via a line interface (Fig. 2, page 4 para. [0068]-[0069]) referenced by the interconnections between the Data Store 205 and the Dataflow chip 202 and ultimate transfer to the Ethernet MAC 203, selected from the group consisting of an Ethernet interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203, a Fast Ethernet Interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 with 10Gb Ethernet, a Gigabit Ethernet interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 with 10x1Gb Ethernet, an OC-48/STM-16 interface (Fig. 2, page 3 para. [0059]) referenced by the Packet Over Sonet interface 203 with 4xOC-48c, an OC-12/STM-14 interface (Fig. 2, page 3 para. [0059]) referenced by the Packet Over Sonet interface 203 with 16xOC-12c. Busso and Gulick do not teach an OC-3/STM-1 interface, an IF Video interface, a DS-1 interface, a DS-3 interface, an E-1 interface and an E-3 interface.

Chow teaches an OC-3/STM-1 interface (Fig. 1, col. 6 lines 7-45) referenced by the OC-3 of 1.6 Gbps Access Shelf 3B, an IF Video interface (Fig. 1, col. 6 lines 7-45) referenced by the FastBus Video of 800Mbps Access Shelf 3C, a DS-1 interface (Fig. 1, col. 6 lines 7-45) referenced by DS-1 of 800Mbps Access Shelf 3D, a DS-3 interface (Fig. 1, col. 6 lines 7-45) referenced by the DS-3 of 800Mbps Access Shelf 3C, an E-1

interface (Fig. 1, col. 6 lines 7-45) referenced by the E-1 of 800Mbps Access Shelf 3D, and an E-3 interface (Fig. 1, col. 6 lines 7-45) referenced by the E-3 of 800Mbps Access Shelf 3C.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Switching Core interfaces of Chowto the Multicast Data Structure of Basso and Gulick for the purpose of maximizing utilization of a switching core by providing a variable number of universal card slots depending on the interface card bandwidth as suggested by Chow (col. 4 lines 50-54).

Claim 38, Busso teaches wherein transmitting said packet data from said storage element (Fig. 2, page 4 para. [0068]-[0069]) referenced by the large Datastore Memory 205 as repository for frames awaiting retransmission and multiple DRAM interfaces to provide sustained transmit and receive bandwidth for the port interface, via a plurality of line interfaces (Fig. 2, page 4 para. [0068]-[0069], Fig. 5, page 5 para. [0084]-[0086]) referenced by the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports and by the interconnections between the Data Store 205 and the Dataflow chip 202 with ultimate transfer to the Ethernet MAC 203, comprises transmitting said packet data from said storage element via a line interface (Fig. 2, page 4 para. [0068]-[0069]) referenced by the interconnections between the Data Store 205 and the Dataflow chip 202 and ultimate transfer to the Ethernet MAC 203, selected from the group consisting of an Ethernet interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC

interface 203, a Fast Ethernet Interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 with 10Gb Ethernet, a Gigabit Ethernet interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 with 10x1Gb Ethernet, an OC-48/STM-16 interface (Fig. 2, page 3 para. [0059]) referenced by the Packet Over Sonet interface 203 with 4xOC-48c, an OC-12/STM-14 interface (Fig. 2, page 3 para. [0059]) referenced by the Packet Over Sonet interface 203 with 16xOC-12c, an OC-3/STM-1. Busso and Gulick do not teach an OC-3/STM-1 interface, an IF Video interface, a DS-1 interface, a DS-3 interface, an E-1 interface and an E-3 interface.

Chow teaches an OC-3/STM-1 interface (Fig. 1, col. 6 lines 7-45) referenced by the OC-3 of 1.6 Gbps Access Shelf 3B, an IF Video interface (Fig. 1, col. 6 lines 7-45) referenced by the FastBus Video of 800Mbps Access Shelf 3C, a DS-1 interface (Fig. 1, col. 6 lines 7-45) referenced by DS-1 of 800Mbps Access Shelf 3D, a DS-3 interface (Fig. 1, col. 6 lines 7-45) referenced by the DS-3 of 800Mbps Access Shelf 3C, an E-1 interface (Fig. 1, col. 6 lines 7-45) referenced by the E-1 of 800Mbps Access Shelf 3D, and an E-3 interface (Fig. 1, col. 6 lines 7-45) referenced by the E-3 of 800Mbps Access Shelf 3C.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Switching Core interfaces of Chowto the Multicast Data Structure of Basso and Gulick for the purpose of maximizing utilization of a switching core by providing a variable number of universal card slots depending on the interface card bandwidth as suggested by Chow (col. 4 lines 50-54).

Allowable Subject Matter

5. Claims 10, 40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Citation of Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Patent number 5903544, Sakamoto et al. discloses a packet handler. Pub. No. 2004/0170176, Kadambi et al. discloses a method for handling IP multicast packets in a network switch.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John L. Shew whose telephone number is 571-272-3137. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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